IN THE ABSTRACT:

Please amend the abstract as shown on the next page:

ABSTRACT

Coherent accesses and updates to state shared by parallel processors, such as ~~SIMD~~ Single Instruction, Multiple Data (SIMD) array processors, is made possible by the use of state elements having local memory storing the state and permitting serialisation of accesses. Operations on single or multiple items of state are ~~perfumed~~ performed by a fixed/hardwired set of operations but they can be programmable by sending command and data to control operations. Individual state elements comprise the local memory, an arithmetic unit, and command and control logic. Multiple state elements are pipelined in state cells which can, in turn, be ~~organised~~ organized into state arrays and state engines effecting complete control over shared state access. A read/modify/write operation can be performed in only two cycles and a complete command in only three to five cycles.